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10/612,608	07/01/2003	Chi-Long Wu	JCLA8671-1	4788

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EXAMINER	
HA, NATHAN W	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,608	WU, CHI-LONG	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,21 and 22* is/are rejected.

7)☒ Claim(s) *17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1a. Claim 17 is objected to because of the following informalities: the element "injectionlayer" should be changed to "injection layer", in claim 17, line 2. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 7-12, 15-16, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Roach, US 6,274,978, mentioned above.

In regard to claim 7, in figs. 1 and 2, Roach discloses a method of fabricating organic electroluminescence panel comprising the steps of:

providing a substrate 110;

forming a plurality of first electrodes 120 (col. 3, line 52) on the substrate, wherein the first electrode includes a driving region (col. 3, lines 50-52 and col. 4, lines 24-25) and at least an interconnection region 140 and the interconnection region is protruded from the driving region (fig. 3);

forming at least a patterned organic electroluminescence panel layer 100 on the

substrate, wherein the patterned organic light-emitting layer exposes the interconnection (fig. 2);

forming a plurality of second electrodes 162 on the organic light-emitting layer; and

forming a plurality of poly solder interconnections 140 on the interconnection region and on the second electrodes.

In regard to claim 8, wherein each of the driving regions of the first electrodes is a stripe (fig. 2).

In regard to claim 9, wherein each of the driving regions of the second electrodes are a stripe (fig. 2).

In regard to claim 10, wherein the extension direction of the first electrodes is perpendicular to the extension direction of the second electrodes (fig. 2).

In regard to claim 11, wherein the material for the first electrodes includes Indium Tin Oxide (ITO) (col. 8, lines 19-20).

In regard to claim 12, wherein the material for the second electrodes include Metal such as aluminum, gold, etc. (col. 9, lines 1-2).

In regard to claims 15 and 16, wherein the formation of the patterned organic light-emitting layer comprises the steps of:

forming an organic light-emitting layer 100; and

defining the organic light-emitting layer to form a plurality of openings and strips thereon, wherein the openings expose the interconnection regions (fig. 5).

In regard to claim 22, Roach discloses wherein the solder interconnections are arranged in area array (fig. 9a).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roach et al. (US 6,274,978, hereinafter, Roach) in view of Fang (US 2003/0127720.)

In regard to claim 1, in fig. 3, Roach discloses a method of fabricating an organic electroluminescence panel package comprising the steps of:

providing a printed circuit board 210 (col. 3, line 61) arranged with a plurality of solder pads 230 (col. 4, line 3);

forming a plurality of bumps 232 (col. 4, line 4) on the solder pads;

providing at least an organic electroluminescence (OEL) panel 20 (col. 3, line 20 and lines 49-50) arranged on the printed circuit board, wherein the organic electroluminescence (OEL) panel comprises a plurality of poly solder interconnections 140 (col. 3, line 53); and

electrically connect the poly solder interconnections and the bumps.

Roach, however, does not expressly disclose that the connection using a reflow process. It should be noted that reflow process is widely used in the art of

semiconductor packaging for making contact between solder connectors since it provide spherical profile of the connector and cost effectiveness. For instance, Fang, in fig. 7, for example, discloses a semiconductor package including substrate 240 solder pad 244 (fig. 6), solder ball 226, a device 210 comprises solder connectors, not numbered. This package is electrically connected by a reflow operation so that the bumps are transformed into mass of lumps having a spherical profile, and better alignment (sections [0025-0026]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a well known process as taught by Fang in Roach so that the bumps are transformed into mass of lumps having a spherical profile, and better alignment.

In regard to claim 6, Roach discloses wherein the solder interconnections are arranged in area array (fig. 9a).

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roach and Fang as applied to claims 1 and 6 above, and further in view of Chapman et al. (US 2004/0056072, hereinafter, Chapman.)

In regard to claim 2, the above combination discloses all of the claimed limitations except the bumps are formed on the solder pads by means of a wire bonding machine.

Chapman, in fig. 8, for example, discloses a semiconductor device including a method of making connection between pad 44 and the wire through the solder bump 42, wherein the bumps are make by a process using wire bonding machine (section [0022]).

This method is widely available at the time of the invention was made, therefore, by using this method the cost of the product can be lowered due to its availability. The method further provides the making of solder bump and the wire connection simultaneously, and further creates conical shape of the connection devices therein (section [0022]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the available machine as taught by Chapman to make connection devices in the above combination in order to lower the cost of the product its availability. The method further provides the making of solder bump and the wire connection simultaneously, and further creates conical shape of the connection devices therein.

6. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roach and Fang as applied to claims 1 and 6 above, and further in view of Iwasaki et al. (US 5,866,950, hereinafter, Iwasaki.)

In regard to claims 3 and 4, the above combination discloses all of the claimed limitations except the solder interconnections are formed by screen printing process. It should be noted that screen printing process is widely used and the most convenient process since solder in the market is in a paste form. For instance, Iwasaki, in fig. 9, discloses a semiconductor package including substrate 7, a device 8. These devices are electrically connected through device 8a and 7a. Device 7a is made of silver paste and formed by a screen printing process to from connections pads (col. 7, lines 7-20.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a well known process such as printing as taught by Iwasaki in order to in taking the advantage of the most well known and the most convenient process since solder in the market is in a paste form.

In regard to claim 5, silver paste is a low re-flow temperature material.

7. Claims 13-14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roach as applied to claims 7-12 and 15-16 above, and further in view of Iwasaki, mentioned above.

In regard to claims 13 and 14, as discussed in claims 3 and 4 above (similar limitations), the above combination discloses all of the claimed limitations except the solder interconnections are formed by screen printing process. It should be noted that screen printing process is widely used and the most convenient process since solder in the market is in a paste form. For instance, Iwasaki, in fig. 9, discloses a semiconductor package including substrate 7, a device 8. These devices are electrically connected through device 8a and 7a. Device 7a is made of silver paste and formed by a screen printing process to from connections pads (col. 7, lines 7-20.)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a well known process such as printing as taught by Iwasaki in order to in taking the advantage of the most well known and the most convenient process since solder in the market is in a paste form.

In regard to claim 21, see the above discussions regarding claim 5, wherein the silver is a low re-flow temperature material.

Allowable Subject Matter

8. Claims 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for the indication of the allowability of the above claims is the inclusion therein, in combination as currently claimed, of the limitation of the method of fabricating a display device including a step of forming a hole injection layer after the formation of the first electrodes but before the formation of the light-emitting layer, and a step of forming an electron transmitting layer between the light-emitting layer and the second electrode after the formation of the organic light-emitting layer but before the formation of the second electrodes.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nathan Ha
November 16, 2004